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# TITLE OF THE INVENTION

STRESS-ADJUSTED INSULATING FILM FORMING METHOD, SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

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## BACKGROUND OF THE INVENTION

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### 1. Field of the Invention

The present invention relates to a stress-adjusted insulating film forming method, a semiconductor device and a method of manufacturing the same and, more particularly, a method of forming stress-adjusted insulating films which are interposed between respective metal interconnection layers upon laminating three or more metal interconnection layers, a semiconductor device employing the stress-adjusted insulating films and a method of manufacturing the same.



### 2. Description of the Prior Art

In recent years, a multilayered interconnection structure in excess of three layers has been needed with the progress of high integration density of the semiconductor device. Upper and lower interconnections and adjacent interconnections are insulated with the interlayer insulating films interposed therebetween. However,

in such multilayered interconnection structure in excess of three layers, it is extremely important to bury narrow interconnection regions while leaving no void therein and also to planarize surfaces of such buried interconnection regions.

In the meanwhile, as for various kinds of insulating films, their characteristics have been known to those skilled in the art, as indicated in Table I below.

Table I

| Type of insulating film | Step coverage | Flatness | Film quality |
|---|---|---|---|
| SOG film | ○ | ○ | X |
| TEOS/$O_3$thermal CVD film | ◎ | ○ | ○ |
| Plasma CVD film | X | X | ○ |
| High density plasma CVD film | ◎ | X | ◎ |

As one of the interlayer insulating films to be formed between multilayered interconnections in excess of three layers, a combination of plural insulating films consisting of an insulating film with good film quality and an insulating film with good step coverage may be employed. For instance, a combination of the plasma CVD film and the TEOS/$O_3$thermal CVD

film or SOG film is often recommended. In other words, as film forming methods, the plasma CVD method and the thermal CVD method or the coating method may be employed in combination.

In addition, since in general the plasma CVD film has good film quality, it can be used by itself as the interlayer insulating film under the assumption that it is followed by planarization such as by the CMP method, etching-back method, etc. Especially, the high density plasma CVD film is suited for such interlayer insulating film application since it has excellent step coverage. In other words, the interlayer insulating film is formed by ECR, ICP, a high density plasma CVD method such as helicon plasma, etc., and then a surface of the interlayer insulating film is planarized by a CMP (Chemical Mechanical Polishing) method or etching-back method.

Combinations of the above various insulating films which can be used as the interlayer insulating film may be summarized as follows. Illustrative examples which have been used as the interlayer insulating films between four-layered interconnections are shown in FIGS. 1A to 1D.

1) Plasma CVD film+SOG film (FIG. 1A)

2) Plasma CVD film+TEOS/$O_3$thermal CVD film (FIG. 1B)

3) Plasma CVD film alone (+CMP) (FIG. 1C)

4) High density plasma CVD film (+CMP) (FIG. 1D)

In the case of 3), because the ordinary plasma CVD film is inferior in step coverage, a single plasma CVD film is scarcely used as the interlayer insulating film.

Meanwhile, the above various insulating films which can be used as the interlayer insulating film undergo stress, as indicated in Table II below.

Table II

| Type of insulating film | Stress |
|---|---|
| SOG film | tensile stress |
| TEOS/O thermal CVD film | tensile stress |
| Plasma CVD film | compressive stress |
| High density plasma CVD film | compressive stress |

However, no account of stress caused in the overall interlayer insulating film structure has been taken up to this time. As a result, the following problems have arisen. That is, in the case of 1) and 2) , tensile stress is in general caused in the interlayer insulating film with good step coverage and flatness, i.e., the SOC film or the thermal CVD film

(TEOS/$O_3$thermal CVD film, etc.). In particular, in the case of thermal CVD film, cracks are generated in the film, as shown in FIG. 2A, if the film thickness is made thick rather than 1.5 $\mu$m. For contrast, if the thickness of the insulating film is made excessively thin, interconnection regions cannot be buried completely by the insulating film to thus generate sharp recesses thereon, as shown in FIG. 2B, so that the interconnection conductive film remains in the sharp recesses and flatness of the insulating film is spoiled.

Accordingly, there are limitations to use of these insulating films as the single interlayer insulating film. Moreover, it is impossible to employ these insulating films as the interlayer insulating film for the multi-layered interconnections in excess of three layers.

In the case of 3) and 4), extremely large compressive stress is applied as a whole to the insulating films. In order to suppress generation of hillock of the interconnections, etc. and generation of electromigration, it is desired to cover the interconnections with the interlayer insulating film with compressive stress. However, too large a compressive stress causes the wafer per se to physically bend, thereby causing problems in manufacturing or problems in device characteristics.

Still further, such a problem has arisen that, if the width of the interconnection is made narrow and chip size is reduced, stress migration is caused due to stress applied to the interconnection during operation of the device. In other words, if excessively large compressive stress is caused in the insulating film which covers the interconnections such as Al film, etc., the interconnections undergo tensile stress along their grain boundaries thus leading to breaking of the interconnection. The greater the number of layers of the multi-layered interconnections, the higher the possibility of breaking of the interconnection.

## SUMMARY OF THE INVENTION

It is an object of the present invention to provide a stress-adjusted insulating film forming method capable of suppressing electromigration and stress migration in Al interconnections, bowing of the wafer, and cracking in interlayer insulating film while maintaining step coverage and flatness of the overall interlayer insulating film, to provide a semiconductor device with good device characteristics and high reliability, and to provide a method of manufacturing the same.

According to the stress-adjusted insulating film forming method of the present invention, an insulating film having a

tensile stress and an insulating film having compressive stress are alternately deposited on a substrate to form the stress-adjusted insulating film consisting of the laminated insulating films.

Therefore, it is possible to adjust the stress of the overall multi-layered insulating films to less than a limit stress value ($+3x10^5$ dyne/cm which is determined from the experiment) not to generate the cracks in the insulating films. It is also possible to adjust the stress of the overall multi-layered insulating times within the stress range so as to avoid curvature of the wafer, degradation in semiconductor device characteristics, etc.

Further, the stress value of the insulating film can be adjusted by adjusting the thickness of the insulating film to be formed, or by changing the type of film forming gas or film forming conditions (e.g., frequency of plasma generating power, bias power applied to the substrate, heating temperature of the substrate, type of gas, flow rate of gas, etc.). Stress of the overall interlayer insulating films can be calculated with good precision by making use of a calculation equation whose good precision has been confirmed experimentally.

According to the semiconductor device and the method of

manufacturing the same of the present invention, the stress-adjusted insulating film (interlayer insulating film) can be formed to cover the interconnection, based on the above stress-adjusted insulating film forming method.

Thereby, generation of cracks in the interlayer insulating film, curvature of the wafer caused by stress, degradation in semiconductor device characteristics, etc. can be prevented by adjusting stress of the interlayer insulating film appropriately. In addition to the above, stress migration and electromigratton of the interconnection, e.g., the aluminum interconnection, can also be prevented by adjusting stress of the interlayer insulating film appropriately.

Moreover, while preventing generation of cracks in the interlayer insulating film, migration of the interconnections, etc., the interconnections can be incorporated into the multi-layered structure via the interlayer insulating film whose stress is adjusted, thereby resulting in a higher integration density of the semiconductor device.

Other and further objects and features of the present invention will become obvious upon an understanding of the illustrative embodiments about to be described in connection with the accompanying drawings or will be indicated in the appended

claims, and various advantages not referred to herein will occur to one skilled in the art upon employing of the invention In practice.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1A to 1D are sectional views each showing an interlayer insulating film laminated structure in the prior art;

FIGS. 2A and 2B are sectional views showing problems caused in the laminated structure according to the prior art;

FIGS. 3A to 3F are sectional views each showing an interlayer insulating film formed according to a first embodiment of the method of the present invention;

FIGS. 4A and 4B are graphs, each showing change in stress due to multilayer stacking of overall interlayer insulating films by virtue of the interlayer insulating film forming method according to the first embodiment of the present invention;

FIGS. 5A and 5B are graphs, each showing change in stress and generation of cracks due to multilayer stacking of overall interlayer insulating films by the interlayer insulating film forming method according to the first embodiment of the present invention;

FIG. 6 is a graph showing change in stress due to multilayer stacking of overall interlayer insulating films by the interlayer insulating film forming method according to the first

embodiment of the present invention before and after humidity absorption;

FIGS. 7A to 7E are graphs, each showing stress adjustment depending upon various film forming conditions in a plasma CVD method according to the first embodiment of the present invention;

FIGS. 8A to 8C are graphs, each showing stress adjustment depending upon various film forming conditions in a thermal CVD method according to the first embodiment of the present invention;

FIGS. 9A to 9C are sectional views each showing an interlayer insulating film laminated structure formed according to a second embodiment of the present invention;

FIG. 10A is a sectional view showing a semiconductor device produced by a method according to a third embodiment of the present invention; and

FIG. 10B is a graph showing measured values and calculation values in relationships between accumulated laminated thickness and accumulated stress generated in laminated insulating films in FIG. 10A.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

Various embodiments of the present invention will be described with reference to the accompanying drawings. It should

be noted that the same or similar reference numerals are applied to the same or similar parts and elements throughout the drawings, and the description of the same or similar parts and elements will be omitted or simplified.

(1) First Embodiment

An experiment made to check a stress compensation effect of the present invention will be explained hereunder.

First, a method of forming a sample used in the experiment will be explained. Seven samples (S1 to S7) having, respectively, the structures shown in FIGS. 3A to 3F have been used.

(Formation of sample S1)

The laminated structure of the sample S1 is shown in FIG. 3A. Characteristics of respective layers in the sample S1 such as type of insulating film, film thickness, total stress, and generation of cracks are indicated in Table III. The insulating film formed by the plasma CVD method will be called a PECVD film (plasma CVD film) hereinafter, and the insulating film formed by the thermal CVD method will be called a THCVD film (thermal CVD film) hereinafter. Further, "total stress" indicated in Table

III means stress generated in the overall insulating films after respective insulating films have been laminated, which is calculated according to an amount of bowing generated after respective insulating films have been laminated on a silicon wafer. The calculation method is based on the literature, i.e., J. Vac. Sci. & Technol. A, Vol. 4, No. 3, May/Jun 1986, pp. 645-649. Similarly, in Tables IV to IX, total stresses have also been calculated according to the same calculation method.

Table III

| Layer (numeral) | Type of insulating film | Film Thickness ($\mu$m) | Total stress (X$10^5$dyne/cm) | Crack Generation |
|---|---|---|---|---|
| 1st layer (22a) | PECVD film | 0.2 | -0.38 | none |
| 2nd layer (23a) | THCVD film | 0.5 | +0.53 | none |
| 3rd layer (22b) | PECVD film | 1.0 | -2.0 | none |
| 4th layer (23b) | THCVD film | 1.45 | -1.4 | none |
| 5th layer (22c) | PECVD film | 0.4 | -5.4 | none |
| 6th layer (23c) | THCVD film | 1.45 | -4.5 | none |
| 7th layer (22d) | PECVD film | 0.4 | -9.0 | none |
| 8th layer (23d) | THCVD film | 1.45 | -8.3 | none |
| 9th layer (22e) | PECVD film | 0.4 | ≤-10.7 | none |

In the above Table III, film forming conditions for the plasma CVD film except for a film forming time are common throughout all laminated layers, and they are set forth hereunder.

Film forming gas

| | |
|---|---|
| (Flow rate sccm) | TMS(15 sccm)+$N_2$0(450 sccm) |
| Pressure | 0.7 Torr |
| Plasma generating power | 150 W |
| Frequency | 13.56 MHz |
| Bias power | 150 W |
| Frequency | 380 kHz |
| Substrate temperature (Film forming temperature) | 330 °C |
| Film forming rate | 150 nm/mm |

Under the film forming conditions defined as above, a silicon oxide film having compressive stress of $-3.3X10^9$ dyne/cm can be formed.

Moreover, film forming conditions of the thermal CVD film except for a film forming time are common in respective layers, which are set forth hereunder.

| | |
|---|---|
| Film forming gas (Flow rate scom) | TEOS(1500 scom) +$0_3$ 5% in $0_2$ 7.5 1) |
| Substrate temperature (Film forming temperature) | 400 $^0$C |
| Film forming rate | 87 nm/min |

Under the film forming conditions defined as above, a silicon oxide film having tensile stress of $+2.2x10^9$ dyne/cm$^2$ can be formed.

As the organic silane to be included in the film forming gas, TMS (trimethoxysilane: $HSi(OCH_3)_3$) or TEOS(tetraethylortho-

silicate: $Si(OC_2H_5)_4$) has been employed in the plasma CVD method and in the thermal CVD method. However, such organic silane may be any alkylsilane or allylsilane (general formula: $R_nSiH_{4-n}$ (n=1 to 4)), alkoxysilane (general formula: $(RO)_nSiH_{4-n}$ (n=1 to 4)), chain siloxane (general formula: $R_nH_{3-n}SiO(R_kH_{2-k}SiO)_mSiH_{3-n}R_n$ (n=1 to 3; k=0 to 2; m≥=0) derivative of chain siloxane (general formula: $(RO)_nH_{3-n}SiOSiH_{3-n}(OR)_n$ (n=1 to 3)), and ring siloxane (general formula: $(R_kH_{2-k}SiO)_m$ (k=1, 2; m≥=2)) (where R is alkyl group, allyl group, or their derivative).

Still further, ozone ($O_3$) or oxygen ($O_2$) has been employed as the oxygen containing gas. However, the oxygen containing gas may be formed of any of $N_2O$, $NO_2$, CO, $CO_2$, and $H_2O$.

(Formation of sample S2)

The laminated structure of the sample S2 is shown in FIG. 3B. Type of insulating film, film thickness, total stress, and generation of cracks in respective layers of the sample S2 are indicated in Table IV.

Table IV

| Layer (numeral) | Type of insulating film | Film thickness ($\mu$m) | Total Stress | Crack Generation |
|---|---|---|---|---|
| 1st layer (22f) | PECVD film | 0.2 | -0.58 | none |
| 2nd layer (23e) | THCVD film | 1.2 | +2.0 | none |
| 3rd layer (22g) | PECVD film | 0.3 | +0.92 | none |
| 4th layer (23f) | THCVD film | 1.5 | +4.0 | none |
| 5th layer (22h) | PECVD film | 0.35 | +2.4 | none |
| 6th layer (23g) | THCVD film | 1.5 | +5.8 | none |
| 7th layer (22i) | PECVD film | 0.35 | +4.0 | generated |
| 8th layer (23h) | THCVD film | 1.5 | +6.7 | remaining |
| 9th layer (22j) | PECVD film | 0.25 | +4.7 | remaining |

In the above Table IV, film forming conditions of the plasma CVD film, other than forming time, are common throughout all laminated layers, and they are set identically in the case where the sample S1 is formed.

Also, film forming conditions of the thermal CVD film, other than forming time, are common in respective layers, and they are set identically to the case where the sample S1 is formed.

(Formation of sample S3)

The laminated structure of the sample S3 is also shown in FIG. 3B. Type of insulating film, film thickness, total stress, and generation of crack respective layers of the sample S3 are indicated in in Table V.

Table V

| Layer (numeral) | Type of insulating film | Film thickness ($\mu$m) | Total Stress | Crack Generation |
|---|---|---|---|---|
| 1st layer (22f) | PECVD film | 0.2 | -0.69 | none |
| 2nd layer (23e) | THCVD film | 1.2 | +2.3 | none |
| 3rd layer (22g) | PECVD film | 0.4 | +0.6 | none |
| 4th layer (23f) | THCVD film | 1.45 | +3.7 | none |
| 5th layer (22h) | PECVD film | 0.4 | +1.5 | none |
| 6th layer (23g) | THCVD film | 1.45 | +5.1 | none |
| 7th layer (22i) | PECVD film | 0.4 | +2.6 | none |
| 8th layer (23h) | THCVD film | 1.45 | +5.3 | none |
| 9th layer (22j) | PECVD film | 0.2 | +3.4 | none |

In the above Table V, film forming conditions of the plasma CVD film, except for film forming time, are the same for all laminated layers, and they are identical to those employed to form sample S1.

Further, film forming conditions of the thermal CVD film, except for forming time, are the same for all respective layers, and they are identical to the case where the sample S1 is formed.

(Formation of sample S4)

The laminated structure of the sample S4 is shown in FIG. 3C. Type of insulating film, film thickness, total stress, and generation of cracks in respective layers of the sample S4 are indicated in Table VI.

Table VI

| Layer (numeral) | Type of insulating film | Film thickness ($\mu$m) | Total Stress | Crack Generation |
|---|---|---|---|---|
| 1st layer (22k) | PECVD film | 0.1 | -0.34 | none |
| 2nd layer (23i) | THCVD film | 1.5 | +3.4 | none |
| 3rd layer (22l) | PECVD film | 0.1 | - | none |
| 4th layer (23j) | THCVD film | 1.6 | +6.8 | generated |

In the above Table VI, film forming conditions of the plasma CVD film, other than film forming time, are the same for all laminated layers and are identical to the case where the sample S1 is formed.

In addition, film forming conditions of the thermal CVD film, other than film forming time, are the same for all respective layers, as in the case where the sample S1 is formed.

(Formation of sample S5)

The laminated structure of the sample S5 is shown in FIG. 3D. The type of insulating film, film thickness, total stress, and generation of cracks in respective layers of the sample SS are indicated in Table VII.

Table VII

| Layer (numeral) | Type of insulating film | Film thickness ($\mu$m) | Total Stress | Crack Generation |
|---|---|---|---|---|
| 1st layer (22m) | PECVD film | 0.1 | -0.34 | none |
| 2nd layer (23k) | THCVD film | 1.5 | +3.4 | none |
| 3rd layer (22n) | PECVD film | 0.1 | - | none |
| 4th layer (23l) | THCVD film | 1.6 | +6.8 | none |

In the above Table VII, film forming conditions of the plasma CVD film, other than film forming time, are the same for all laminated layers and are set to be identical to the case where the sample S1 is formed.

In addition, film forming conditions of the thermal CVD film, other than film forming time, are the same for all respective layers and are set to be identical to the case where the sample S1 is formed.

(Formation of sample S6)

The laminated structure of the sample S6 is shown in FIG. 3E. Type of insulating film, film thickness, total stress, and generation of cracks in respective layers of the sample S6 are indicated in Table VIII.

Table VIII

| Layer (numeral) | Type of insulating film | Film thickness ($\mu$m) | Total Stress | Crack Generation |
|---|---|---|---|---|
| 1st layer (22p) | PECVD film | 0.1 | -3.2 | none |
| 2nd layer (23m) | THCVD film | 1.2 | -0.65 | none |
| 3rd layer (22q) | PECVD film | 0.1 | - | none |
| 4th layer (23n) | THCVD film | 1.7 | +2.7 | none |

In the above Table VIII, film forming conditions of the plasma CVD film, other than film forming time, were the same for all the respective layers, and were identical to the case where the sample S1 was formed.

In addition, film forming conditions of the thermal CVD film, other than film forming time, were the same for all layers and were set identical to the case where the sample S1 was formed.

(Formation of sample S7)

A laminated structure of the sample S7 is shown in FIG. 3F. Type of insulating film, film thickness, total stress, and generation of cracks in respective layers of the sample S7 are indicated in Table IX.

Table IX

| Layer (numeral) | Type of insulating film | Film thickness ($\mu$m) | Total Stress | Crack Generation |
|---|---|---|---|---|
| 1st layer (22r) | PECVD film | 1.3 | -3.9 | none |
| 2nd layer (23p) | THCVD film | 0.5 | -0.17 | none |

In the above Table IX, film forming conditions for the plasma CVD film, other than film forming time, are the same for all laminated layers and are identical to the case where the sample S1 is formed.

In addition, film forming conditions of the thermal CVD film, other than film forming time, are the same for all layers and are identical to the case where the sample S1 is formed.

The results are shown in FIGS. 4A and 4B for the samples S1 to S3, respectively, based on stress values indicated in above Tables III to V after respective insulating layers have been laminated.

FIG. 4A is a graph showing the cumulative laminated film thickness as the ordinate, on a linear scale and the number of laminated layers as the abscissa. FIG. 4B is a graph showing the stress value ($x10^5$ dyne/cm) on a linear scale as the ordinate and

the number of laminated layers as the abscissa.

As shown in FIGS. 4A and 4B, it is feasible to adjust stress of the overall interlayer insulating films by adjusting respective film thicknesses of the PECVD film and the THCVD film. If the thicknesses of the PECVD films are large relative to the THCVD films, as in sample S1, compressive stress is dominant overall. On the contrary, if the THCVD films are made thicker than the PECVD films as in samples S2 and S3, tensile stress is dominant overall. In the case of the samples S1, S3, even through the film thickness exceeds 7 $\mu$m, cracking is avoided by adjusting stress of overall interlayer insulating films appropriately.

In the sample S2, cracks from when the seventh layer PECVD film 221 is formed continuously after the sixth layer THCVD film 23g has been laminated. The cracks form in all the laminated insulating films. The experiment suggests that, evidently if tensile stress exceeds a certain threshold stress value, cracks are generated. From the experiment, it may be deduced that the threshold stress value to avoid the cracks is 4 to $6 \times 10^5$ dyne/cm. In the sample S2, the reason why no crack formed even though stress has already exceeded $5.8 \times 10^5$ dyne/cm immediately after lamination of the sixth insulating layer, but cracks were formed even though stress has already reduced after lamination of the

seventh insulating layer is considered to be as follows. That is, cracking barely appears in the sixth layer THCVD film 23g since stress in the sixth layer THCVD film 23g has been relaxed to some extent because of its humidity absorption, nevertheless stress may be increased locally in the THCVD film 23g due to dehydration of the THCVD film 23g since the THCVD film 23g is exposed to plasma irradiation during forming the seventh layer PECVD film 22i.

FIGS. 5A and 5B show change in overall stress in the samples S4 to S6 respectively based on the stress values indicated in above Tables VI to VIII versus number of layers laminated.

FIG. 5A is a graph of cumulative laminated film thicknesses as the ordinate ($\mu$m) on a linear scale versus the number of laminated layers as the abscissa. FIG. 5B is a graph of stress as the ordinate (x $10^5$ dyne/cm) on a linear scale versus the number of laminated layers as the abscissa.

As shown in FIGS. 5A and 5B, three samples S4 to S6 are directed to the case where the THCVD films are made thicker than the PECVD films. The cracks appear In the samples S4 and S5, but no crack appears in the sample S6. In this case, like FIGS. 4A and 4B, it may be deduced that the threshold stress value to

avoid forming cracks is 4 to $6X10^5$ dyne/cm. From another experiment, it has been deduced that the stress range for avoiding generation of cracks is less than $+2x10^5$ dyne/cm if the insulating film is formed on an Al film.

In addition, the results are shown in FIG. 6 when change in stress is investigated in the samples S2 to S7 respectively before and after humidity absorption after the multiple insulating layers are laminated.

FIG. 6 is a graph showing the average stress value ($10^9$ dyne/$cm^2$) caused in the laminated films on a linear scale as the ordinate and the time interval before and after humidity absorption as the abscissa. In the above experiment, it seems that ambient humidity of the sample has been about 40% and that humidity absorption has occurred mainly in the thermal CVD films.

From FIG. 6, it is evident that variation in stress due to humidity absorption was largest in samples S4 to S7, in which the uppermost layer is formed of the THCVD film, as compared to the samples S2, S3, in which the uppermost layer is formed of the PECVD film. The stress has been shifted towards the compressive stress side due to humidity absorption in the samples S4 to S7. It is desired that the uppermost layer should be formed of the PECVD film if suppression of variation in stress is needed.

Otherwise, from another experiment, it has been confirmed that plasma irradiation after film formation is effective to suppress variation in stress.

It has been found from the above experimental results that overall stress can be calculated according to the following equation. That is,

$$\text{Stress in overall laminated films } (\delta_T) = \sum_{i=1}^{n} (t_i \times \delta_i)$$

Where n is the total number of laminated films, $t_i$ is a thickness of i-th insulating film (cm), and $\delta_i$ is stress in i-th insulating film (dyne/cm$^2$). As for type of stress of the insulating film, it is assumed that the tensile stress is positive and the compressive stress is negative.

It has been confirmed that, under the assumption that a stress value $\delta$ of the plasma CVD film is $-3\times10^9$ dyne/cm$^2$ and a stress value $\delta$ of the thermal CVD film is $+2\times10^9$ dyne/cm$^2$, stress values calculated according to the above equation exactly coincide with measured stress values, as indicated in Tables III to IX.

From the samples S2, S4, S5, it is understood that a stress range to avoid generation of the cracks is less than about $+3\times10^5$

dyne/cm. If stress of the silicon oxide film formed by the thermal CVD method is assumed as $2x10^9$ dyne/cm$^2$, this corresponds to about 1.5 $\mu$m in terms of the thickness of the silicon oxide film formed by the thermal CVD method.

Therefore, if stress of the overall laminated films calculated by the equation is set to a stress limit ($+3x10^5$ dyne/cm on an Si film, or $+2x10^5$ dyne/cm on an aluminum film) and then thickness and stress of individual insulating films are determined not to exceed this stress limit, cracks in the interlayer insulating films can be prevented.

Depending upon the film forming method and the film forming conditions, stress in the insulating film formed by the plasma CVD method and stress in the insulating film formed by the thermal CVD method can be adjusted as explained hereunder.

For instance, stress in the insulating film formed by the plasma CVD method can be adjusted according to type of gas, flow rate of gas, frequency of plasma generating power, bias power applied to the substrate, film forming temperature, etc. Experimental examples are shown in FIGS. 7A to 7E. Although a TEOS+$0_2$ system reaction gas has been employed in the experimental examples, stress may be adjusted in a similar manner when a TMS+$N_2O$ system reaction gas is employed.

Also stress in the insulating film formed by the thermal CVD method can be adjusted according to type of gas, flow rate of gas (including ozone concentration in oxygen), film forming temperature, film forming rate, etc. Experimental examples are shown in FIGS. 8A to 8C. The TEOS+$O_3$ reaction gas has been employed here as the film forming gas.

Usually, stress in the insulating film formed by the thermal CVD method is often shifted to the compressive stress side because of humidity absorption after formation. Therefore, if moisture is removed from the insulating film by plasma irradiation, stress in the insulating film can be shifted to the tensile stress side. As a result, it is possible to stabilize stress in the insulating film.

(2) Second Embodiment

FIGS. 9A to 9C are sectional views showing combinations of the insulating films constituting interlayer insulating films according to a second embodiment of the present invention.

FIG. 9A shows a structure wherein insulating films 14a, 14b and an insulating film 15a are laminated alternatively on a substrate 101 by the plasma CVD method and the thermal CVD method, respectively. The substrate 101 consists of a ground

insulating film 12 formed on a semiconductor substrate 11 and an interconnection layer 13 formed on the ground insulating film 12.

In the structure of FIG. 9A, since thicknesses of the PECVD films 14a, 14b are large, compressive stress becomes dominant in the stress of the whole of the laminate when calculated according to the above equation. Thus, generation of the cracks can be prevented. In the event that it is expected not to excessively increase the absolute value of compressive stress, a lower limit of stress (lower limit of the compressive stress) in the whole laminate according to the equation as well as an upper limit thereof (upper limit of the tensile stress to suppress generation of the cracks) is defined, and then thicknesses and stress of the PECVD films 14a, 14b and the THCVD film 15a must be selected so that the overall stress is within the range between the upper limit and the lower limit.

FIG. 9B shows a structure wherein insulating films 15b, 15c by the thermal CVD method and an insulating film 14c by the plasma CVD method are laminated alternatively on the substrate 101 in a reverse order to that in FIG. 9A.

In the structure of FIG. 9B, since thicknesses of the THCVD films 15b, 15c are large, tensile stress becomes dominant in the stress of the overall laminate when calculated according to the

above equation. The thicknesses and stress of the PECVD film 14c and the THCVD films 15b, 15c may be selected so as to adjust stress in the overall laminate according to the equation below the upper limit of the tensile stress beyond which the cracks generate. Consequently, generation of the cracks can be prevented.

FIG. 9C shows a structure wherein impurity-free silicon oxide film (NSG film) 15d and an impurity containing insulating film 16, which includes at least one of phosphorus and boron, are laminated alternatively on the substrate 101 by the thermal CVD method. PSG film, BPSG film, or BSG film used as the impurity containing insulating film 16 has tensile stress of about $+5X10^8$ dyne/$cm^2$.

Calculation according to the equation provides tensile stress as stress in the overall laminate. However, such tensile stress can be reduced by inserting the impurity containing insulating film 16 in contrast to the case where only the impurity non-containing silicon oxide films (NSG film) 15d are laminated. Therefore, in case the thickness of the interlayer insulating film is desired to be made especially thick, such thickness can be made larger by inserting the impurity containing insulating film 16 appropriately into the interlayer insulating films in contrast to the case where the interlayer insulating

film is formed of the NSG film only.

In the above structure, although the interlayer insulating film has been constituted by the insulating films of a three-layered structure, the insulating films of two-layered structure or four-layered structure or more may be adopted. In addition, although the one-layered interconnection has been employed, plural-layered interconnections can be laminated and then the above interlayer insulating films can be interposed between the interconnections.

(3) Third Embodiment

A semiconductor device and a method of manufacturing the same according to a third embodiment of the present invention will be explained with reference to FIG. 10A hereinbelow. FIG. 10A shows an example in which four interconnection layers are formed. The interlayer insulating films formed according to the method of manufacturing the interlayer insulating film of the present invention are interposed respectively between adjacent interconnection layers. Film forming gas and film forming conditions used in the plasma CVD method and the thermal CVD method are selected identically to those explained in forming the sample S1 in the first embodiment.

As shown in FIG. 10A, interconnections 33a, 33b made of an aluminum film having a thickness of 0.7 μm are formed on a substrate 31.

First, a silicon oxide film 34a of 0.2 μm thickness is formed by the plasma CVD method to cover the interconnections 33a, 33b.

Then, a silicon oxide film 35a of 0.5 μm thickness is formed on the silicon oxide film 34a by the thermal CVD method.

In turn, a silicon oxide film 34b of 0.9 μm thickness is formed on the silicon oxide film 35a by the plasma CVD method.

Subsequently, a surface of the silicon oxide film 34b is planarized by polishing the silicon oxide film 34b by the CMP method (Chemical Mechanical Polishing Method). Thereby, formation of the first-layered interlayer insulating film 1L having a thickness of 1.6 μm to cover the first-layered interconnections 33a, 33b is completed.

Next, second-layer interconnections 33c, 33d made of an aluminum film having a thickness of 0.95 μm are formed on the planarized silicon oxide film 34b.

Then, a second-layer interlayer insulating film 2L having a thickness of 1.85 μm is formed by repeating the above steps. The second-layer interlayer insulating film 2L consists of a silicon oxide film 34c of 0.1 μm thickness formed by the plasma CVD method, a silicon oxide film 35b of 0.45 μm thickness formed by the thermal CVD method, and a silicon oxide film 34d of 1.3 μm thickness formed by the plasma CVD method.

Then, third-layer interconnections 33e, 33f made of an aluminum film having a thickness of 0.95 μm and a third-layer interlayer insulating film 3L having a thickness of 1.85 μm are formed in this order on the second-layer interlayer insulating film 2L. The third-layer interlayer insulating film 3L consists of a silicon oxide film 34e of 0.1 μm thickness formed by the plasma CVD method, a silicon oxide film 35c of 0.45 μm thickness formed by the thermal CVD method, and a silicon oxide film 34f of 1.3 μm thickness formed by the plasma CVD method.

Then, fourth-layer interconnections 33g, 33h made of an aluminum film having a thickness of 0.95 μm and a fourth-layered covering insulating film 4L having a thickness of 1.85 μm are formed in this order on the third-layer interlayer insulating film 3L. The covering insulating film 4L consists of a silicon oxide film 34g of 0.1 μm in thickness formed by the plasma CVD method, a silicon oxide film 35d of 0.45 μm thickness formed by

the thermal CVD method, and a silicon oxide film 34h of 1.3 $\mu$m thickness formed by the plasma CVD method.

Thus, four interconnection layers, three interlayer insulating films 1L to 3L which are interposed respectively between adjacent interconnection layers, and the covering insulating film 4L for covering the fourth layer interconnection are formed. The preselected interconnections of the interconnections are connected through via holes (not shown) formed in the interlayer insulating films 1L to 3L, into which conductors are buried.

Change in cumulative stress of the semiconductor device formed as above is shown in FIG. 10B.

FIG. 10B is a graph showing relationships between measured values and calculation values for stress and cumulative laminate thickness and accumulated stress generated in laminated insulating films in FIG. 10A. In FIG. 10B, the ordinate shows the cumulative laminate thickness ($\mu$m) on a linear scale and the abscissa shows stress values (x($10^5$ dyne/cm)) on a linear scale. The reason why measuring points do not coincide with the layer number is that the adjacent silicon oxide films 34b and 34c, 34d and 34e, 34f and 34g which are formed by the plasma CVD method are each regarded as one point, respectively.

According to the results shown in FIG. 10B, in the multilayered structure formed similarly as the actual semiconductor device, the measured values substantially coincide with the calculated values in relationships between cumulative laminate thickness and cumulative stress in the insulating films. The reason why no crack appears in the insulating film even when cumulative stress has exceeded the stress limit of $3x10^5$ dyne/cm defined in the first embodiment, will now be explained. Because the actual stress limit is considerably high rather than $3x10^5$ dyne/cm but the stress limit is reduced to a smaller value if abnormal defects are caused in the insulating film, nevertheless the stress limit should be selected so as not to generate cracks in such a abnormal case.

According to the above, if stress of the overall laminated interlayer insulating films, etc. 1L to 4L is set not to exceed the stress limit ($3x10^5$ dyne/cm on the insulating film, $2x10^5$ dyne/cm on the aluminum film), an arbitrary number of interconnections can be laminated without generating cracks in respective interlayer insulating films.

If the above stress limits are restricted, i.e. made narrower, generation of cracks can be suppressed much more, and the curvature of the wafer, degradation in the semiconductor device characteristics, etc. due to stress can also be prevented,

and further stress migration or electromigration of the interconnection, e.g., aluminum interconnection, can be prevented.

In addition, if multilayered interconnections are laminated via the stress-adjusted interlayer insulating films while avoiding formation of cracks in the interlayer insulating film, etc. and electromigration of the interconnection, etc., a semiconductor device having a high integration density can be obtained.

Stress in the insulating film formed on the interconnections 33a to 33h has not been measured or calculated in the above disclosure. Since, as described above, the thickness and the stress limits of the insulating film are different on the interconnections 33a to 33h and on regions in which the interconnections 33a to 33h are not formed, stress in respective regions must be calculated individually to correspond to the thickness according to the equation derived in the first embodiment, and then the thickness must be determined to suppress the stress in the respective regions to within the preselected stress range.

As described earlier, according to the interlayer insulating film forming method of the present invention, multiple

insulating layers whose total stress is adjusted can be formed by laminating insulating films having different stress mixedly on the substrate.

Accordingly, it is possible to adjust the stress of the overall multilayered insulating films to less than the limit stress value so as not to generate cracks in the insulating film, and to adjust the stress of the overall multilayered insulating films to within the stress range so as not to cause curvature of the wafer, degradation in the semiconductor device characteristics, etc. due to stress.

Further, the stress value of the insulating film can be adjusted by adjusting the thickness of the insulating film to be formed, or by adjusting type of film forming gas or film forming conditions. In this case, stress of the overall interlayer insulating films can be calculated with good precision by making use of a calculation equation whose good precision has been confirmed experimentally.

According to the semiconductor device and the method of manufacturing the same of the present invention, the interlayer insulating film whose stress is adjusted can be formed to cover the interconnection, based on the above interlayer insulating film forming method.

Consequently, generation of cracks in the interlayer insulating film, curvature of the wafer because of stress, degradation in semiconductor device characteristics, etc. can be prevented by adjusting stress of the interlayer insulating film appropriately. In addition to the above, stress migration and electromigration of the interconnection, e.g., the aluminum interconnection, can also be prevented by adjusting stress of the interlayer insulating film appropriately. Moreover, while preventing generation of cracks in the interlayer insulating films, migration of the interconnections, etc., the interconnections can be laminated via the interlayer insulating films whose stress is adjusted, thereby obtaining a higher integration density for the semiconductor device.

Various modifications will become possible for those skilled in the art after receiving the teachings of the present disclosure without departing from the scope thereof.